Electronically Tunable Multi-Line TRL Using an Impedance Matched Multi-Bit MEMS Phase Shifter

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***Abstract*—An electronically tunable thru-reflect-line (TRL) calibration set that utilizes a 4-b true time delay microelectromechanical systems (MEMS) phase shifter topology, based on impedance-matched slow-wave coplanar waveguide (CPW) sections, is presented. The accuracy of the tunable TRL is close to a conventional multi-line TRL calibration and shows a maximum error bound of 0.12 at 40 GHz. Experimental data for a 4.6 mm-long tunable delay standard shows 317°/dB phase shift at 50 GHz (or 91°/mm) with S_{11} less than −21 dB from 1–50 GHz. The MEMS beams on the phase shifter are actuated using high resistance SiCr bias lines with typical actuation voltage around 30–45 V.**

***Index Terms*—Electronic calibration, microelectromechanical systems (MEMS) phase shifter.**

I. Introduction

CONSIDERABLE effort has been made to develop accurate techniques for calibrating vector network analyzers (VNAs) based on the use of space conservative standards [1]. The multi-line thru-reflect-line (TRL) method is very accurate for broad band calibration [2]; however the required use of two or more delay lines can lead to inefficient utilization of wafer surface area. Space conservative calibration methods such as the SOLT, LRM, and LRRM provide accuracy that is close to a multi-line TRL, provided that broad band models for the standards are available. An alternative to reducing the footprint of standards is to use an electronic phase shifter that can represent multiple delay lines by changing its phase state. It is very important that there be minimal variation in the effective characteristic impedance between different phase shifter states, since the delay lines ideally differ only in transmission phase and loss. An added advantage of the electronic calibration approach is that a minimal number of probe placements is necessary, thereby minimizing this aspect of calibration error.

True time delay (TTD) distributed micro electro-mechanical (MEM) transmission lines (DMTLs) are a proven solution for high performance, low loss phase shifters. A DMTL usually consists of a uniform length of high impedance coplanar waveguide (CPW) that is loaded by periodic placement of discrete MEM capacitors [3]–[5]. The increase in the distributed capacitance when the MEM capacitor is electrostatically actuated (down-state) provides a differential phase shift ($\Delta\phi$) with respect to the phase in the nonactuated state (up-state).

A problem with loaded-line phase shifters is that the amount of phase shift is proportional to the difference in the loaded and unloaded impedances, thus restricting the achievable $\Delta\phi$ per unit length in light of impedance matching considerations. To overcome this limitation, a new true time delay MEMS phase shifter topology was presented in [6]. The topology uses cascaded, switchable slow-wave CPW sections to achieve high return loss in both states, a large $\Delta\phi$ per unit length, and phase shift per dB that is comparable to a uniform 50 Ω transmission line. The goal of this letter is to demonstrate the new phase shifter topology in a multi-bit configuration to realize the thru and delay lines of a TRL calibration set ("tunable TRL"). Experimental results for the 4-b phase shifter that is 4.6 mm-long demonstrate S_{11} less than −21 dB through 50 GHz with $\Delta\phi$/dB of approximately 317°/dB (or 91°/mm) at 50 GHz (described in Section II). In Section III, the 4-b phase shifter is used to realize the line standards (thru and four delay lines) and the accuracy of the tunable TRL is compared with a standard multi-line TRL on two substrates using the calibration comparison method. The calibrations are also validated by measuring other DUTs, and it is shown that the vector error difference between the S-parameter data is less than the predicted error bounds. To the best of authors' knowledge this is the first reported results that utilize MEMS based on-wafer tunable TRL calibration.

II. Four-Bit Slow-Wave Phase Shifter

The 4-b phase shifter shown in Fig. 1 consists of ten cascaded slow-wave unit cells and is designed to provide small variations in the impedance around 50 Ω on a 500 μm thick quartz substrate (ε_r =3.78, $\tan\delta$ =0.0004). The states of the phase shifter designed in this work provide $\Delta\phi$ of 45°, 90°, 180°, and 225° at 35 GHz. The performance of the unit cell and a fabrication process for the unit cell are presented in [6].

Measurements of the unit cell were performed from 1–50 GHz using a Wiltron 360B VNA and 150-μm pitch GGB microwave probes. A multi-line TRL calibration was performed using conventional calibration standards fabricated on the wafer.

Fig. 2 shows the measured S_{11} for the phase shifter in all the states while Fig. 3 shows the measured $\Delta\phi$ and worst case S_{21} (dB) for the 4-b phase shifter. It is shown in Fig. 3 that S_{21} in all states is greater than −1 dB and the measured $\Delta\phi$ is within 5% of the designed value. When comparing the results for S_{21} of the

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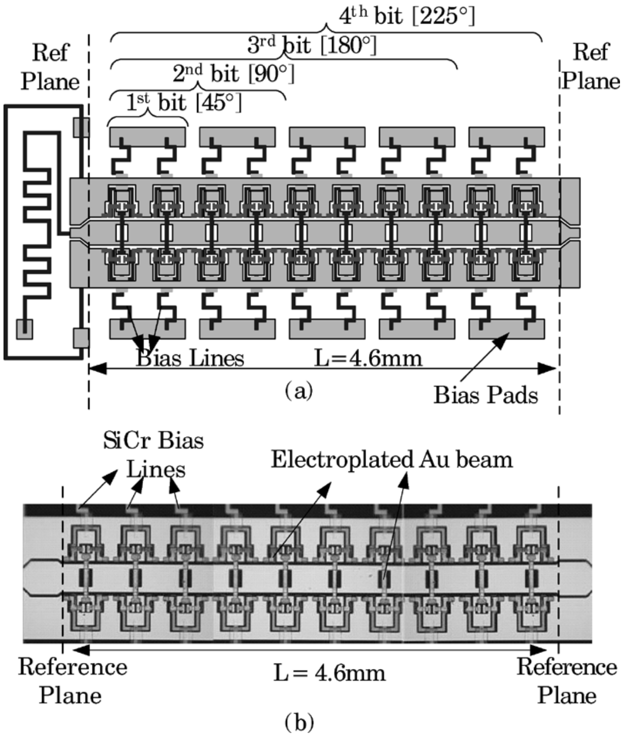

Fig. 1. (a) Schematic of the 4-b MEM slow-wave phase shifter. (b) Photograph of the fabricated device.

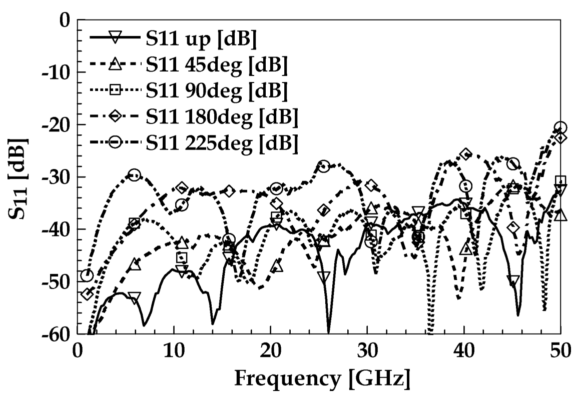

Fig. 2. S_{11} of the 4-b slow wave MEM phase shifter in all states.

4-b phase shifter with a uniform CPW line of the same electrical length, it was found that the loss was within -0.35 dB at 50 GHz (measured S_{21} after a TRL calibration for a uniform 50 Ω line is -0.61 dB). Furthermore, measured S_{11} for the phase shifter is less than -21 dB through 50 GHz indicating good impedance match. The extracted effective impedance from the measured results is within 2% of 50 Ω (51.1 Ω–49.1 Ω for all the states).

III. Tunable Multi-Line TRL

The MEMS tunable 4-b phase shifter presented herein is used to realize four delay line calibration standards in a multi-line TRL. The normal-mode operation (or $\Delta\phi = 0°$) of the phase shifter mimics the thru standard. The different bits of the slow-wave phase shifter are actuated in order to emulate the delay line standards. The open standard is realized using a separate, uniform CPW line. The effective offset lengths of the delay lines extracted from measured $\Delta\phi$ at 35 GHz are approximately 739 μm

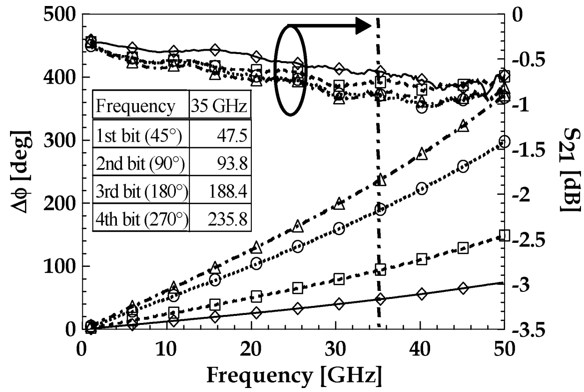

Fig. 3. $\Delta\phi$ and S_{21} for the 4-b phase shifter.

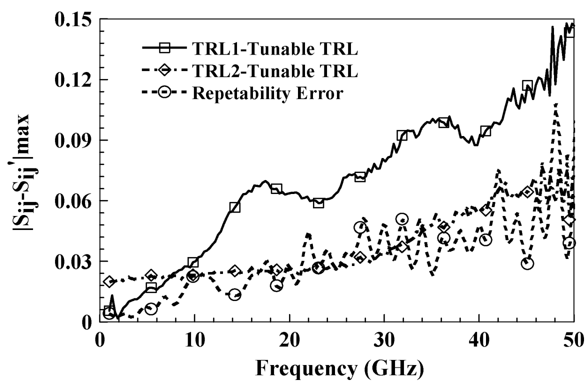

Fig. 4. Upper bound error $|S_{ij} - S'_{ij}|_{max}$ between standard TRL and tunable TRL.

($\Delta\phi = 47°$), 1460 μm ($\Delta\phi = 93°$), 2931 μm ($\Delta\phi = 188°$), and 3669 μm ($\Delta\phi = 235°$).

The results of a tunable TRL calibration are compared with a calibration performed using uniform CPW line standards on the quartz substrate. The reference planes for both calibrations are established at the probe tips with Z_0 corrected to 50 Ω. Furthermore, same number of line standards was used in both the calibrations. The maximum error bound $|S_{ij} - S'_{ij}|_{max}$ between multi-line TRL standard on quartz (TRL1) and tunable-TRL on quartz is computed using the calibration comparison method [1]. The comparison was also made between standard TRL on a CS-5[1] substrate (TRL2) and the tunable TRL, as illustrated in Fig. 4.

The calibration comparison method is based on the assumption that a perfect multi-line TRL calibration using conventional standards calculates the true scattering parameters S_{ij} of a device from uncorrected measurement data. However, an imperfect TRL calibration based on standards with errors (tunable TRL) will result in calibration coefficients which differ from those of the perfect calibration. These imperfect calibration coefficients calculate scattering parameters S'_{ij}, which differ from the actual scattering parameters S_{ij}. The calibration-comparison method determines an upper bound for $|S_{ij} - S'_{ij}|$ from differences in the perfect and imperfect calibration coefficients when $|S_{ii}| < 1$ and $|S_{12}\ S_{21}| < 1$. The upper bounds indicate the

[1]CS-5 is a commercial calibration substrate manufactured by GGB Industries, Naples, FL.

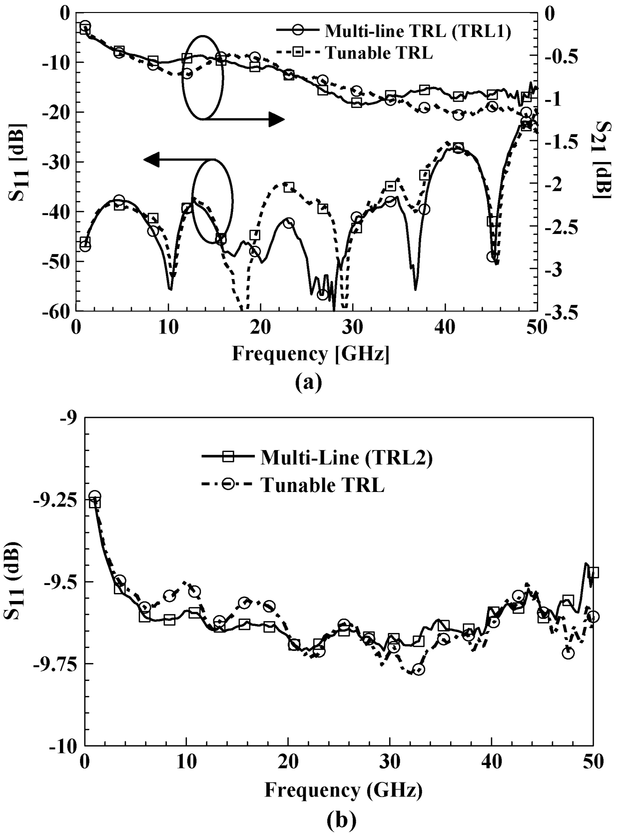

Fig. 5. (a) S_{11} and S_{21} of 9 mm long verification structure. The line was measured after a tunable TRL calibration and a standard TRL on quartz (TRL1). (b) S_{11} of a 25-Ω load verification structure on a 700-μm thick CS-5 substrate.

maximum possible difference in any of the four S-parameters for a two-port passive device.

It is seen from Fig. 4 that the upper bound between TRL1-tunable TRL and TRL2-tunable TRL increases linearly with a maximum bound of 0.14 at 50 GHz for TRL1-tunable TRL calibration sets. The increase in the error bound is due to the slight increase in the insertion loss and a 2% deviation from 50 Ω for the 4-b phase shifter when compared to uniform CPW line. For completeness, the repeatability of the two multi-line TRL calibrations on the quartz substrate is also shown in the figure.

IV. Validation

A. 9 mm Long Delay Line Standard on Quartz Substrate

A 9-mm-long uniform CPW line was measured after performing a tunable TRL and a TRL1. It is seen from Fig. 5(a) that the measurement results performed using the tunable TRL and TRL1 agree well. Furthermore, the maximum vector difference between the two measured S-parameters is within the estimated error bounds.

B. 25-Ω Load on a CS-5 Substrate

A 25-Ω load verification structure was measured on 700 μm thick CS-5 substrate ($\varepsilon_r = 9.9$, $\tan\delta = 0.002$) after performing a on-wafer calibration (TRL2) using uniform CPW line standards. It is seen from Fig. 5(b) that the measurement results performed using tunable TRL and TRL2 agree well and the maximum vector difference between the S-parameters is within the predicted error bound.

V. Conclusion

In this letter, a true-time-delay 4-b CPW phase shifter operating from 1–50 GHz is presented that utilizes slow-wave MEMS sections. Experimental results for a 4-b phase shifter that is 4.6 mm-long demonstrate S_{11} less than -21 dB through 50 GHz with $\Delta\phi$/dB of approximately 317°/dB (or 91°/mm) at 50 GHz. An electronically tunable calibration is made possible by realizing all the line standards using the multi-bit phase shifter in a typical multi-line TRL. The calibration comparison method shows a maximum bound of 0.14 at 50 GHz between a tunable TRL calibration and a standard multi-line TRL on two different substrates. The tunable TRL method provides for an efficient usage of wafer area while retaining the accuracy associated with the TRL technique, and reduces the number of probe placements from five to two (with potentially no change in probe separation distance).

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