

Three-Dimensional, W-Band Circuits Using Si Micromachining

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Abstract — This paper presents results from the development effort of Si micromachined three-dimensional high density circuits for W-band operation. Measurements of the performance of a power distribution network in a multilayer environment show that on-wafer packaging improves performance and allows for high density integration, small size, and considerably reduced cost.

I. INTRODUCTION

High density microwave packaging efforts for next generation airborne and space-based phased array antenna radars began in 1993. Cofired ceramic technologies were chosen to implement the packaged modules due to process maturity and mechanical strength of the materials [1]. Although this technology has resulted in high density circuits operating at frequencies as high as Ka-band, it has provided very costly solutions which do not have satisfactory circuit performance due to parasitic package effects. To avoid these problems, and provide the capability for higher integration, higher operating frequencies, and better performance; silicon (Si) micromachining has recently been identified as an enabling technology to provide novel and cost effective solutions. The mechanical, thermal, and electrical properties of high resistivity Si compare well with the best ceramics thus making it an appropriate substrate for this type of application. Si micromachining has been used to improve the performance of conventional transmission lines [2, 3, 4]. Not only has circuit performance increased, but size has drastically reduced due to the capability to shield the circuit on-wafer. On-wafer packaging has been successfully demonstrated in simple circuits up to W-band [5], but herein is extended to fairly complex circuit environments. With the recent advancements in vertical transition designs, the capability to create multilayer

high density Si micromachined circuits is now becoming a reality.

The work presented herein is part of a 3-D high density Si micromachined “power cube” linear array transmit module for W-Band applications. The objective of this program is to generate 1-2 W/in² at W-band with a low cost, Si micro-package. The cube features, flipped InP MMIC amplifiers, novel single layer vertical interconnects, low loss CPW-to-microstrip transitions, soft-bump wafer-to-wafer interconnections, and compact on-wafer packaged power distribution networks.

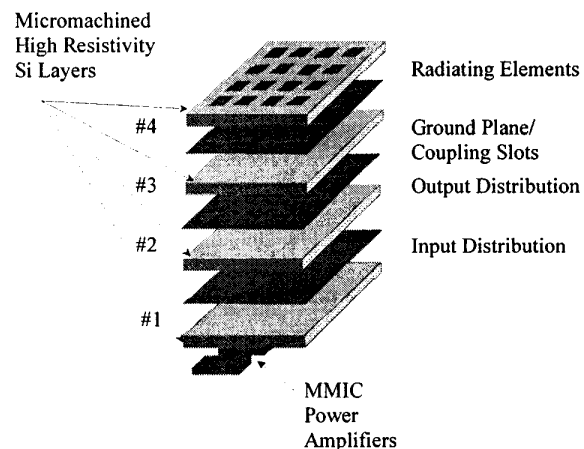


Fig. 1. Concept of Si micromachined “power cube” tile module.

The interconnect lines are packaged on-wafer using micromachined cavities and are designed to provide high performance operation, free of parasitic modes that may be caused by neighboring conducting planes (see Fig. 1:

Ground plane/coupling slots). Advancements in this technology will help meet performance, cost, weight, and size requirements more effectively.

Table 1: Function of power cube layers

Layer	Si	Metal
1	Heat sink/MMIC access	Input distribution
2	Si micromachined layer/ Carries on-wafer packaging cavities	Output distribution
3	Si micromachined layer/ Carries on-wafer packaging cavities	Antenna feed
4	Antenna/Micromachined layer for reduction of surface waves	Patch antenna array

This paper presents the development of the high performance distribution network based on a finite ground coplanar (FGC) waveguide interconnect architecture. It specifically focuses on the performance and packaging issues for the output distribution network used in the power cube (See Fig. 1: Output distribution).

This network is comprised of multiple bends, impedance steps, tees and Wilkinson dividers. Individual component performance is critical to feed network efficiency and for this reason geometry optimization for the lowest insertion and return loss has been pursued.

II. POWER DISTRIBUTION LAYOUT

The power cube is made of separate Si wafers each one responsible for a separate function as listed in Table 1. The W-band signal is amplified by four MMICs flipped to the lower part of the vertical structure and is then distributed vertically to 16 radiating elements via four 1 x 4 distribution networks (see Fig. 1, Layers 3 and 4) Each antenna element is $750 \times 750 \mu\text{m}^2$ and is separated $850 \mu\text{m}$ from an adjacent one. The total area available for distributing power to the antenna feed layer is $6 \text{ mm} \times 6 \text{ mm}$ thus requiring high line density but with non-compromised performance (see Fig. 2). For this reason, a compact FGC line with total width equal to $300 \mu\text{m}$ has been chosen as the interconnect (see Fig. 3). In the FGC network, airbridges have been included to suppress unwanted mode excitation at discontinuity. To preserve the integrity of the airbridges

when bonding the layers, micromachined packages are monolithically developed along with the circuits.

The antenna array layout requires that the separation between ground planes in the adjacent 1 x 4 distribution networks be $80 \mu\text{m}$ in some locations (Fig. 2). While it is true that fields in FGC lines concentrate in the aperture regions, measurements indicate coupling levels as high as -26 dB in this arrangement. By adding upper shielding cavities that conform to the circuit shape, the coupling can be reduced to -40 dB .

A $40 \mu\text{m}$ cavity is etched into the next level Si wafer (Fig. 1, Layer 3) which supports the feeds to the antennas. The antennas are fed by a microstrip line, through an H-shape slot which requires a continuous conductor plane. Two line geometries are shown in Fig. 3 with continuous conductor metal. The unpackaged line will be compared to the packaged one to determine how lower metal presence affects complex FGC circuits.

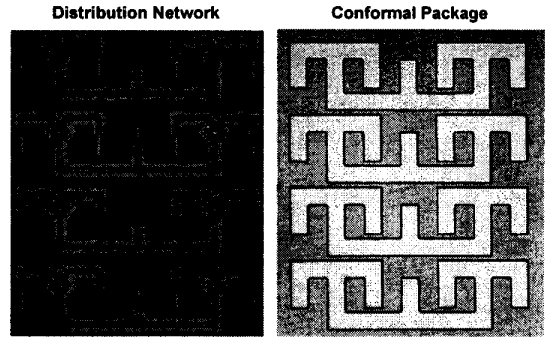


Fig. 2. Photograph of distribution network and conformal package. Ground-to-ground spacing between networks is $80 \mu\text{m}$ (Layers 2 and 3 in Fig. 1).

III. DESIGN AND FABRICATION

A center conductor width of $40 \mu\text{m}$, aperture width of $24 \mu\text{m}$, and ground plane width of $106 \mu\text{m}$ are used to realize a 50Ω line on $100 \mu\text{m}$ -thick Si. The tee and Wilkinson dividers are standard equal division 50Ω designs with air-bridge step compensations to improve circuit response [6]. Tantalum nitride (TaN) thin-film resistors are part of the Wilkinson design (100Ω) and 50Ω termination resistors are included at three of the four output ports in order to take two port measurements.

The distribution network is fabricated on high-resistivity bare Si ($>2000 \Omega\text{-cm}$). 700 \AA of TaN ($R_s=45\Omega/\text{sq}$) is sputtered onto the substrate and selectively etched using reactive ion etching (RIE) for the resistor metal. 9500 \AA of

gold (Au) is evaporated for the circuit metal and 3 μm Au airbridges are electroplated to equalize the ground planes.

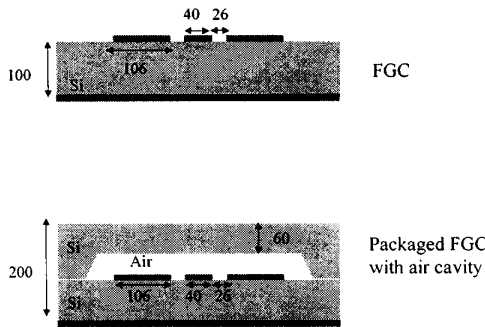


Fig. 3. Cross-section of unpackaged and packaged FGC lines with a continuous conducting plane.

The shielding cavity is fabricated on a 100 μm -thick Si substrate with 8500 \AA SiO_2 masking layer. In order to take on-wafer measurements, probe access windows are required. The cavities and access windows are defined using photolithography and etched in a two-step process with EDP solution [2]. The metal conductor on the cavity wafer is 2000 \AA evaporated Au. Alignment marks and windows are printed and etched on the distribution and cavity wafers, respectively. The two wafers are mechanically aligned and bonded with silver epoxy [7].

IV. PERFORMANCE

The single distribution network arrangement for two-port measurements is shown in Fig. 4. The S-Parameters for the distribution network have been measured using a HP8510C Network Analyzer, with 100 μm -pitch GGB Picoprobes. On-wafer TRL calibration standards are used with NIST's Multical program [8] to calibrate the system. Looking at the two port measurement path for a single distribution network, there are two right-angle bends and approximately 1.5 mm of transmission line length designed with the tee and Wilkinson divider.

Measured data for the single components are listed in Table 2. The tee with bend circuit (Fig. 5) represents the input of the distribution network and the Wilkinson with bend (Fig. 6) represents the output network. These measured values highlight the best performance insertion loss within the frequency range of 90-95 GHz. Results show that the performance in the packaged circuit was substantially better than that of the unpackaged circuit. It is worth noticing that unpackaged circuits demonstrate a varying performance due to parasitic effects that are sensitive to circuit environment (See Table 2).

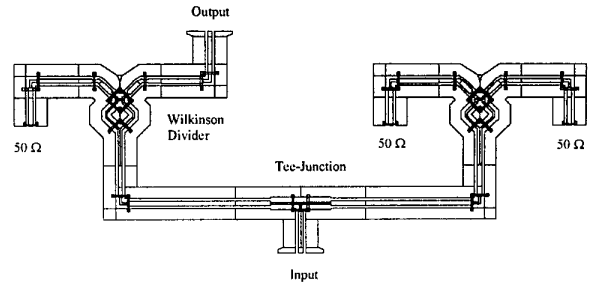


Fig. 4. Single distribution network for two-port measurements.

Measurements of the 1 x 4 network are shown in Figs. 7 and 8 for two FGC lines (Fig. 3). Results indicate the minimum loss for the packaged structure as -0.7 dB, a value close to the total loss in Table 2. The measurement error is approximately 0.1-0.2 dB and is attributed to probe contact repeatability due to thin circuit metal ($< 1 \mu\text{m}$). The presence of the ground plane and neighboring circuits degrade the performance of the unpackaged FGC structure (see Fig. 8).

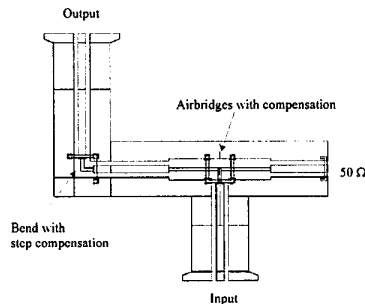


Fig. 5. Tee with right-angle bend for input of distribution network.

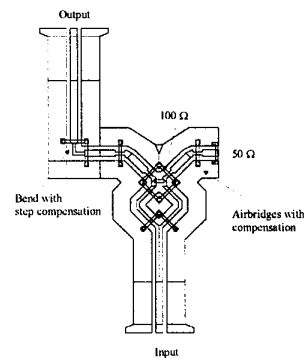


Fig. 6. Wilkinson power divider with right-angle bend for output of distribution network.

V. CONCLUSIONS

As indicated by the measurements, the packaged FGC line out-performed the unpackaged line due to the elimination of parasitic modes caused by conducting planes printed in close proximity (see Fig. 1) The presented results strongly demonstrate superior performance starting with the individual components and following with the distribution network. Specifically, this technology realized Wilkinson power dividers with insertion loss near -0.25 dB, and less than -0.2 dB for bends and tees. Finally, the 1 x 4 distribution network has demonstrated an insertion loss of approximately -0.7 dB around the design frequency (94 GHz) indicating an efficiency of 85%. These results indicate the capability of this technology to provide superior integration options in addition to achieve excellent performance compared to any other planar technology.

Table 2: Measured loss of individual components.

Component (Peak performance)	With Package (dB)	Without Package (dB)
Tee	~-0.19	-0.4 -0.6
Wilkinson	~-0.25	-0.6 -1
Transmission line loss	~-0.26	~-0.25
Total Loss	~-0.7	-1.25 -2

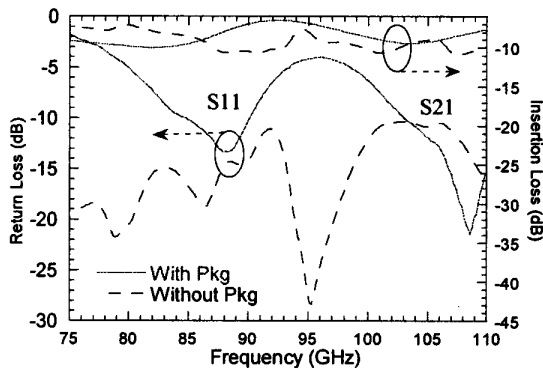


Fig. 7. Measured S-Parameters of distribution network, with and without packaging.

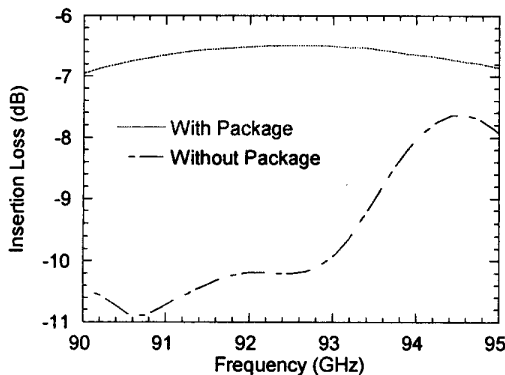


Fig. 8. Measured insertion loss of distribution network, with and without packaging.

ACKNOWLEDGMENTS

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REFERENCES

- [1] J. A. Reddick, et. al., "High Density Microwave Packaging Program Phase 1-- Texas Instruments/Martin Marietta Team," in *IEEE MTT-S Digest*, pp. 173-176, 1995.
- [2] R. F. Drayton, R. M. Henderson, and L. P. B. Katehi, "Advanced Monolithic Packaging Concepts for High Performance Circuits and Antennas," in *IEEE MTT-S Digest*, pp. 1615-1618, 1996.
- [3] .T. Weller, et. al., "Optimization of MM-Wave Distribution Networks Using Silicon-Based CPW," in *IEEE MTT-S Digest*, pp. 537-540, 1998.
- [4] K.J. Herrick, et. al., "W-Band Micromachined Finite Ground Coplanar (FGC) Line Circuit Elements," in *IEEE MTT-S Digest*, pp. 269-272, 1997.
- [5] S.V. Robertson, et. al, "W-Band Microshield Low-Pass Filters," in *IEEE MTT-S Digest*, pp. 625-628, 1994.
- [6] T. Weller, et. al., "Experimental Results on Microshield Line Circuits," in *IEEE MTT-S Digest*, pp. 827-830, 1993.
- [7] R. F. Drayton and L.P.B. Katehi, "Development of Self-Packaged High Frequency Circuits Using Micromachining Techniques," *IEEE Trans. on Microwave Theory and Techniques*, vol. 43, no. 9, pp. 2073-2080, Sept. 1995.
- [8] R. B. Marks and D. F. Williams, Program MultiCal, rev. 1.00, NIST, August, 1995.